

MEMORY CELL

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of International Patent Application Serial No. PCT/DE02/02759, filed July 26, 2002, which published in German on February 27, 2003 as WO 03/017374 A2, and is incorporated herein by reference in its entirety.

5 FIELD OF THE INVENTION

The invention relates to a memory cell.

BACKGROUND OF THE INVENTION

Computers with memory arrays are used in a wide variety of applications including mainframe computers, personal computers, washing machines, kitchen appliances, motor
10 vehicles, telephones, answering machines and other applications. A computer is to be understood here in the widest sense as an electronic control device and/or computing device.

The memory arrangement of a computer is used for permanently or temporarily storing data, for example parameters which are necessary for operating the computer, or
15 computing results which are generated by the computer when the computer is operating.

The memory arrangement has a memory with at least one memory cell, generally a plurality of memory cells. Each memory cell has a storage element in which a quantity of
electrical charge can be stored in order to set the memory contents of the memory cell.

There are volatile and non-volatile memory cells. In a volatile memory cell, a
20 memory content which is stored in the storage element typically remains for only approximately a second in the storage element. The memory contents must therefore be periodically refreshed. In a non-volatile memory cell, the memory contents which are stored in the storage element remain permanently in the storage element for a storage time

of the order of magnitude of years.

A non-volatile MOSFET-based memory cell (MOSFET = metal oxide semiconductor field effect transistor) is based on a MOSFET with a source region, a drain region, a channel region running between the source region and the drain region, a gate electrode (control gate) which is arranged in order to control the channel region, and a gate oxide layer which is arranged between the gate electrode (control gate) and the channel region.


In the non-volatile MOSFET-based memory cell, the gate electrode is used as a control gate. A storage element for storing memory contents of the memory cell is provided between the control gate and the gate oxide layer over the channel region. The storage element has a potential barrier both with respect to the channel region and with respect to the control gate. As a result of the fact that a suitable electrical voltage which is sufficiently high in terms of absolute value is applied to the control gate, electrical charge carriers can be charged from the channel region into the storage element, or can be discharged from the storage element into the channel region. As a result, memory contents of the memory cell can either be programmed or erased.

An example of a non-volatile memory is the EEPROM (Electrically Erasable Programmable Read Only Memory). In an EEPROM, programmed memory contents can be erased again by applying an electrical voltage.

Non-volatile MOSFET-based memory cells are, in terms of design, floating gate memory cells and MIOS memory cells (MIOS = metal insulator oxide semiconductor).

In a floating gate memory cell the storage element is formed by a metallicity conductive floating gate.

In a MIOS memory cell, the storage element is formed from an insulator storage element made of (at least) one insulator material. The memory contents of the storage

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density, i.e., to accommodate as much individual memory content items per unit area or per unit volume.

For this purpose, the structure size of each individual memory cell is typically reduced.

5 U.S. Patent No. 6,335,554 B1 discloses a non-volatile semiconductor memory in which a first gate region section which is arranged above a first ONO storage layer and above a source region, a second gate region section which is arranged above a second ONO storage layer and above a drain region, and a third gate region section which is arranged above a channel region and above a gate-insulating layer are provided, the first,
10 second and third gate region sections being electrically connected to one another.

In addition, DE 10036911 A1 (application date: 28 July 2000, date laid-open: 14 February 2002) proposes a memory cell with two ONO storage layers, one of which adjoins a source region and the other a drain region. The conductivity of a channel region is controlled by means of a gate region which is arranged over it as well as by means of
15 two lateral gate components which are connected to the gate region via a connecting line, a gate-insulating layer being arranged between the channel region and the gate region.

SUMMARY OF THE INVENTION

The invention is based on the problem of providing an efficient and reliable memory cell which is economical in terms of current.

20 The problem is solved by means of a memory cell having the features according to the independent patent claim.

A memory cell is provided which has:

a substrate,

a source region formed in the substrate,

25 a drain region formed in the substrate,

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a channel region provided between the source region and the drain region and having a variable electrical conductivity,

a source-end control gate extending at least partially over a source-end edge section, which adjoins the source region, and being designed to change the electrical conductivity of the source-end edge section,

a drain-end control gate extending at least partially over a drain-end edge section, which adjoins the drain region, and being designed to change the electrical conductivity of the drain-end edge section,

an injection gate arranged between the source-end control gate and the drain-end control gate and extending over a central section of the channel region, the injection gate being electrically isolated from the drain-end control gate and designed to change the electrical conductivity of the central section, which extends between the source-end edge section and the drain-end edge section of the channel region,

a source-end storage element extending at least between the source-end edge section and the source-end control gate,

a drain-end storage element extending at least between the drain-end edge section and the drain-end control gate, and

a gate oxide arrangement having at least one gate oxide layer extending between the substrate on the one side and the source-end control gate, the drain-end control gate and the injection gate on the other side,

wherein the source-end control gate and the drain-end control gate are electrically connected to one another.

It is possible to store separate memory contents, and thus one bit of data, in the source-end storage element and in the drain-end storage element respectively. In this way, the storage capacity in the memory cell is doubled in comparison to that of a memory cell

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dioxide layer, and a second silicon dioxide layer which is formed on the silicon nitride layer.

The gate oxide layer and the first silicon dioxide layer can be formed as separate layers. Alternatively, the gate oxide layer can be formed in one piece with the first silicon
5 dioxide layer.

Contact can be made with the source-end control gate and the drain-end control gate separately. This is advantageous if different electrical voltages are to be applied to the source-end control gate and the drain-end control gate.


The source-end control gate and the drain-end control gate are preferably
10 electrically connected to one another. In this case, in total only one voltage source is necessary for the source-end control gate and the drain-end control gate to apply a respective voltage. In addition, in this way, a particularly simple and thus efficient programming of the memory cell can be achieved. For example, the drain-end storage element can be programmed first, then the polarity of the source drain voltage can be
15 reversed and then the source-end storage element can be programmed without further changes, as has already been explained above. Alternatively, the source-end storage element can be programmed first, and then the drain-end storage element.

The channel region can have an n-type channel. Alternatively, the channel region can have a p-type channel.

20 A memory array according to the invention, which is embodied as an EEPROM, has at least one memory cell which is constructed as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

The exemplary embodiments of the invention are illustrated in the figures and will be explained in more detail below; of said figures:

25 Fig. 1 shows a memory cell according to a first embodiment of the invention in
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which the drain-end storage element is programmed;

Fig. 2 shows the memory cell from Fig. 1 in which the memory contents of the source-end storage element and of the drain-end storage element are erased;

Fig. 3a shows a memory cell according to a second embodiment of the invention in cross section in a first fabrication state during its manufacture;

Fig. 3b shows the memory cell according to the second embodiment of the invention in cross section in a second fabrication state during its manufacture;

Fig. 3c shows the memory cell according to the second embodiment of the invention in cross section in a third fabrication state during its manufacture;

Fig. 3d shows the memory cell according to the second embodiment of the invention in cross section in a fourth fabrication state during its manufacture;

Fig. 3e shows the memory cell according to the second embodiment of the invention in cross section in the completed fabrication state; and


Fig. 3f shows two memory cells according to the invention, the same as that shown in Fig. 3e, from above.

DETAILED DESCRIPTION OF THE PREFERRED MODE OF THE INVENTION

Fig. 1 shows a memory cell according to a first embodiment of the invention in which the drain-end storage element is programmed.

The memory cell from Fig. 1 has a substrate 100, an n^+ -type doped source region 101 formed in the substrate 100, an n^+ -doped drain region 102 formed in the substrate 100, and an n-type channel region 103 which runs between the source region 101 and the drain region 102 and has a variable electrical conductivity.

The memory cell also has a source-end control gate 104 which extends at least partially over a source-end edge section 105, adjoining the source region 101, of the channel region 103, and is designed to change the electrical conductivity of the source-end

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edge section 105.


The memory cell also has a drain-end control gate 106 which extends at least partially over a drain-end edge section 107, adjoining the drain region 102, of the channel region 103 and is designed to change the electrical conductivity of the drain-end edge section 107.

An injection gate 108 which extends over a central section 109 of the channel region 103 and is designed to change the electrical conductivity of the central section 109 is arranged between the source-end control gate 104 and the drain-end control gate 106. The central section 109 extends here between the source-end edge section 105 and the drain-end edge section 107 of the channel region 103.

The memory cell also has a source-end storage element 110 made of silicon nitride which extends between the source-end control gate 104 on the one hand, and the injection gate 108, the source-end edge section 105 and the source region 101 on the other.

In addition, the memory cell has a drain-end storage element 111 made of silicon nitride which extends between the drain-end control gate 106 on the one hand, and the injection gate 108, the drain-end edge section 107 and the drain region 102 on the other.

The memory cell also has a gate oxide arrangement 112 made of silicon dioxide. The gate oxide arrangement 112 has a gate oxide layer 113 which extends between the substrate 100 on the one hand, and the source-end control gate 104, the drain-end control gate 106 and the injection gate 108 on the other. A layer made of silicon dioxide is provided between the source-end control gate 104 and the source-end storage element 110, between the source-end storage element 110 and the injection gate 108, between the injection gate 108 and the drain-end storage element 111 and between the drain-end storage element 111 and the drain-end control gate 106, respectively, these layers made of silicon dioxide forming a part of the gate oxide arrangement 112 and being formed in one

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piece with the gate oxide layer 113.

The process of the programming of the drain-end storage element 106 is described below.

An electrical voltage of 0 V is applied to the source region 101. An electrical
5 voltage of 5 V is applied to the drain region. An electrical voltage of 10 V is applied to
the source-end control gate 104 and to the drain-end control gate 106 by means of a
common voltage source. An electrical voltage of 1.5 V is applied to the injection gate
108. As a result, electrical charge carriers (electrons) are injected from the source region
101 into the source-end edge section 105 of the channel region 103. Owing to the
10 relatively low voltage at the injection gate 108, only a low current flows in the central
section 109 of the channel region 103. Owing to the high voltage at the drain-end control
gate 106, electrical charge carriers (electrons) are charged into the drain-end storage
element 111 and trapped there.

A memory cell according to an alternative embodiment of the invention has a
15 p⁺-type doped source region, a p⁺-type doped drain region and a p-type channel region
which runs between the source region and the drain region and has a variable electrical
conductivity.

Fig. 2 shows the memory cell from Fig. 1 in which the memory contents of the
source-end storage element 110 and of the drain-end storage element 111 are deleted.

20 The same positive electrical voltage of 5 V is applied to the source region 101 and
to the drain region 102. The same negative electrical voltage of -5 V is applied to the
source-end control gate 104 and to the drain-end control gate 106. An electrical voltage of
0 V is applied to the injection gate 108. As a result, holes are charged from the channel
region 103 into the source-end storage element 110. These holes recombine with negative
25 electrical charge carriers trapped in the source-end storage element 110. As a result, the
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negative electrical charge of the negative charge carriers which are trapped in the source-end storage element 110 are compensated, thus causing the memory contents in the source-end storage element 110 to be erased. In an analogous way, holes from the channel region 103 are charged into the drain-end storage element 111. As a result, the negative electrical charge of the electrical charge carriers trapped in the drain-end storage element 111 are compensated, thus causing the memory contents in the drain-end storage element 111 to be erased. In order to promote the discharging of the storage elements 110, 111, a negative electrical voltage can alternatively be applied to the injection gate 108.

In order to read out the memory contents (bits) stored in the source-end storage element 110, an electrical voltage of 1.2 V can be applied between the source region 101 (0 V) and the drain region 102 (1.2 V). A voltage of approximately 2 V is then applied to the source-end control gate 104, to the drain-end control gate 106 and to the injection gate 108, respectively. In order to read out the memory contents (bits) stored in the drain-end storage element 111, an electrical voltage of -1.2 V is applied between the source region 101 (1.2 V) and the drain region 102 (0 V). The voltages at the source-end control gate 104, at the drain-end control gate 106 and at the injection gate 108 are also 2 V, i.e., only the polarity of the source drain voltage is reversed.


The following table 1 shows typical electrical voltages which are to be applied to the different elements of the memory cell and which are suitable, in the combination given, for programming, erasing or reading out the memory cell.

305 are formed, as shown in Fig. 3c, is carried out on the structure from Fig. 3b. A channel region extends between the source region 304 and the drain region 305. In each case a layer made of thick oxide 306 is then formed over the source region 304 and the drain region 305 by means of oxidation so that the structure shown in Fig. 3c is formed.

5 The nitride spacers 303 are then removed by means of a wet etching step. In this wet etching step, a silicon dioxide layer acts as an etch stop layer so that the gate oxide layer 301 is not attacked and the structure shown in Fig. 3d is formed.

As shown in Fig. 3e, starting from the structure from Fig. 3d, a silicon dioxide etching step, in which the gate oxide layer 301 is removed in regions 307 next to the injection gate 302 (and the thick oxide 306 thinned out), is firstly carried out. Then, a lower oxide layer 308 made of silicon dioxide is formed on the surface of the partially fabricated structure. A storage element layer 309 made of silicon nitride is formed on the lower oxide layer 308. An upper oxide layer 310 made of silicon dioxide is formed on the storage element layer 309. The lower oxide layer 308, the storage element layer 309 and the upper oxide layer 310 form an ONO layer (ONO = Oxide-Nitride-Oxide) in each of the regions 307 next to the injection gate 302 so that a source-end storage element 311 and a drain-end storage element 312 are formed. The source-end storage element 311 and the drain-end storage element 312 are each formed from the storage element layer 309 made of silicon nitride, and are bounded on the one side by the lower oxide layer 308 and on the other side by the upper oxide layer 310.

A polysilicon layer 313, which is doped in situ, is formed on the upper oxide layer 310. A tungsten silicide layer 314 is formed on the polysilicon layer 313. The polysilicon layer 313 and the tungsten silicide layer 314 are patterned photolithographically (photolithography and subsequent etching of the layers 313, 314), and the photolithographic resist is subsequently stripped (removed). In this way, a source-end

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control gate 315 and a drain-end control gate 316 are formed from the polysilicon layer 313 and the tungsten layer 314. The source-end control gate 315 and the drain-end control gate 316 are electrically connected to one another.

Fig. 3e shows the finished memory cell in cross section.

5 Fig. 3f shows, for the sake of further clarification, two memory cells according to the invention which are arranged one next to the other and are the same as that shown in Fig. 3e, from above.

In alternative embodiments of the memory cell according to the invention, the substrate 100, 300 is an n-type substrate. In this case, the channel region has a p-type
10 channel.